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09/834,954	04/16/2001	Tomohide Terashima	57454-062	5366

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	#7

DATE MAILED: 06/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/834,954	Applicant(s) TERASHIMA, TOMOHIDE
	Examiner Johannes P Mondt	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on ____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-13* is/are pending in the application.

4a) Of the above claim(s) ____ is/are withdrawn from consideration.

5)☐ Claim(s) ____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-13* is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on ____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on ____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. ____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). ____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

Upon request by Applicant the examiner has again included the signed Information Disclosure Statement.

Response to Amendment

Amendment A filed 4/9/2 has been entered as Paper No. 6. The examiner has considered Amendment A prior to this Office Action. In Amendment A all claims have been substantially amended. Comments on "Remarks" in Amendment A shall therefore be restricted to points of relevance to the new claims.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. ***Claims 2-3 and 11*** are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular: when the third impurity region is stipulated by claims 2 and 11 to be (a) formed on the surface of the semiconductor layer and (b) surrounded by the first impurity region, then it is physically impossible for any electrode parts formed on the surface of said semiconductor layer to be so configured as to cause the first impurity region to be sandwiched between it and

the third semiconductor region. All electrode parts shown by Applicant are formed on the surface of said semiconductor layer. Claim 3 is also rejected, because it depends on rejected claim 2.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1, 4 and 9*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno et al (5,895,939) in view of Hwang et al (EP-0252173 A1).

With regard to claim 1: Ueno et al teach a semiconductor device (title, abstract) including:

a semiconductor substrate having a main surface (Figure 6) (comprising n+ region); a semiconductor layer 63 (column 9, line 63) of first conductivity type (n- region) formed on the main surface of said semiconductor substrate; a first buried impurity region (marked "n") of first conductivity type formed between said semiconductor layer and semiconductor substrate; a second buried impurity region 70 (cf. column 10, line 3) formed between said first buried impurity region and said semiconductor layer; a first impurity region 65 (cf. column 9, line 62) of second conductivity type formed in the surface of said semiconductor layer; a second impurity region 64 (cf. column 9, lines 64-65) of first conductivity type

formed in the surface or inside said semiconductor layer located in a region above said second buried impurity region; and a semiconductor element which includes said first impurity region and said second impurity region and which has a switching function (cf. abstract, first sentence) formed on the surface of said semiconductor layer, wherein the withstanding voltage is secured by a depletion layer extending from an interface between said second buried impurity region and said semiconductor layer under the condition where said semiconductor element is turned OFF (cf. abstract); and said second buried impurity region includes a first gap part (gap between the two regions marked 70 in Figure 6) wherein said second buried impurity region is disconnected.

Ueno does not necessarily teach the first impurity region of second conductivity type 65 to be electrically connected to said second buried impurity region 70. However, it would be obvious to provide said electrical connection in order to prevent the possibility of breakdown due to parasitic capacitance between regions 65, 63, and 70. Among many other sources, by Hwang et al, for the specific case immediately related to the invention by Ueno, i.e., a vertical field effect transistor: see abstract, final sentence, and Example 1, page 17. The inventions are combinable, because to provide an electrical connection between regions is standard in the semiconductor device art. Motivation to do so stems from the obviously deleterious effects of parasitic capacitance. Reasonable success in attempts to combine the inventions is justified, considering the long experience in successfully combatting parasitic capacitance.

With regard to claim 4: Figures 3A,B in Ueno provide examples in which additional impurity regions of the second kind are formed on a surface of said semiconductor layer.

With regard to claim 9: the junction interface between said first buried impurity region and said second buried impurity region as taught by Ueno is indeed uneven (cf. Figure 6).

3. ***Claim 6*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno and Hwang et al as applied to claim 1 above, and further in view of Hirano (EP-0817387A1), or, in the alternative, in view of Lin et al (6,348,714). Ueno nor Hwang et al necessarily teach the further limitation of claim 6. However, it would be obvious to include more than one gap in the semiconductor device according to claim 1 in the standard application of MOSFET devices in series, as for instance is carried out to create a voltage-level shifter, as shown by Hirano (see Derwent abstract, for instance), because then each sub-unit would have to be protected against parasitic capacitance. Alternatively, Lin et al teach a plurality of buried impurity regions 116 separated by gaps so as to combat body effects such as kink effect (cf. column 1, lines 28-37 and column 2, lines 20-57) so as to provide for body contacts at various positions for better results in combatting these effects through the spatial distribution (see also column 4, lines 28-40).

4. ***Claim 7*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno and Hwang et al and either Hirano or, in the alternative, Lin et al as applied to claim 6

above, and further in view of Lin et al (not necessary as additional references in the aforementioned alternative). It is inherent to separated and imperfect conducting regions (impurity regions in this case) to be floating.

5. ***Claim 8*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno and Hwang et al as applied to claim 1 above, and further in view of Galbiati et al (5,629,558). Neither Ueno nor Hwang et al necessarily teach the further limitation defined by claim 8. However, such recess away would be of obvious advantage since the effective thickness of the epitaxial layer would thereby be increased, resulting in a corresponding increase in breakdown voltage, which is the basis of the invention by Galbiati et al (cf. abstract and column 1, lines 48-58). It thus would have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to stipulate the further limitation of claim 8.

6. ***Claims 10 and 12-13*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito (6,051,457). Ito (cf. Figure 2(h) and column 5, lines 1-25) teaches a semiconductor device including: a semiconductor substrate having a main surface; a semiconductor layer of first conductivity type (n type) 32 formed on the main surface of said semiconductor substrate; a buried impurity region of first conductivity type 18 formed between said semiconductor layer and semiconductor substrate; a first impurity region of first conductivity type 34(1) formed on the surface of said semiconductor layer and electrically connected to said buried impurity region (regions 34(1), 32, and 18 abut and are of the same conductivity type, therefore they are electrically connected); a second impurity region of second conductivity type (p type) 26 on the surface of said

semiconductor layer located in a region above said buried impurity region; and a semiconductor element which includes said first impurity region and said second impurity region (cf. title and abstract: said semiconductor element being an integrated circuit with passive component and ESD device); and said buried impurity region includes a gap part wherein said buried impurity region is disconnected (hole or gap filled with impurity region 16(1); column 5, line 16).

Ito does not necessarily teach said device to have a switching function and operate in depletion mode. However, Ito does teach in another embodiment a device identical to the one described above as applied to a transistor (cf. Figure 4), while depletion mode transistors are common in the art, as witnessed by Chevalier who teaches a depletion mode transistor (claims 2, 4, and 42) over a buried well (cf. Figure 7).

With regard to claim 12: the semiconductor element of Ito includes an additional (there are only two impurity regions mentioned in claim 10, so why is this impurity region called "fourth" is puzzling) impurity region 28 of second type formed in the surface of said semiconductor layer.

With regard to claim 13: said gap is in a direction to which the depletion layer extends normally in the event of application to a field effect transistor as taught by Chevalier.

Response to Arguments

All claims have been substantially altered; hence response to arguments by Applicant is limited to those aspects relevant for the newly amended claims. The new

claim aspect introduced is the gap in one of the buried regions. This gap certainly is covered by the disclosure through Figures 17-18 and related discussion, but constitutes an essential part of another embodiment from those covered in the original claim language. Consequently, new art can be cited to reject the present newly amended claims.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
June 3, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800